AF & IFW

PTO/SB/17 (10-03)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE


# FEE TRANSMITTAL for FY 2004

*Effective 10/01/2003. Patent fees are subject to annual revision.*

☐ Applicant Claims small entity status. See 37 CFR 1.27

**TOTAL AMOUNT OF PAYMENT** ($) 330.00

| *Complete if Known* | |
|---|---|
| Application Number | 09/904,042 |
| Filing Date | 07/11/2001 |
| First Named Inventor | Han, K. Michael |
| Examiner Name | Wojciechowicz, Edward J. |
| Art Unit | 2815 |
| Attorney Docket No. | 0180129 |

## METHOD OF PAYMENT *(check all that apply)*

☐ Check ☒ Credit card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account

Deposit Account Number: 50-0731

Deposit Account Name: Farjami & Farjami LLP

**The Director is authorized to:** *(check all that apply)*

☐ Charge fee(s) indicated below ☒ Credit any overpayments

☒ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

## FEE CALCULATION

### 1. BASIC FILING FEE

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description | Fee Paid |
|---|---|---|---|---|---|
| 1001 | 770 | 2001 | 385 | Utility filing fee | |
| 1002 | 340 | 2002 | 170 | Design filing fee | |
| 1003 | 530 | 2003 | 265 | Plant filing fee | |
| 1004 | 770 | 2004 | 385 | Reissue filing fee | |
| 1005 | 160 | 2005 | 80 | Provisional filing fee | |

SUBTOTAL (1) ($)

### 2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

| | | Extra Claims | | Fee from below | | Fee Paid |
|---|---|---|---|---|---|---|
| Total Claims | -20**= | | X | | = | |
| Independent Claims | -3**= | | X | | = | |
| Multiple Dependent | | | | | = | |

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description |
|---|---|---|---|---|
| 1202 | 18 | 2202 | 9 | Claims in excess of 20 |
| 1201 | 86 | 2201 | 43 | Independent claims in excess of 3 |
| 1203 | 290 | 2203 | 145 | Multiple dependent claim, if not paid |
| 1204 | 86 | 2204 | 43 | **Reissue independent claims over original patent |
| 1205 | 18 | 2205 | 9 | **Reissue claims in excess of 20 and over original patent |

SUBTOTAL (2) ($)

** or number previously paid, if greater; For Reissues, see above

## FEE CALCULATION (continued)

### 3. ADDITIONAL FEES

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description | Fee Paid |
|---|---|---|---|---|---|
| 1051 | 130 | 2051 | 65 | Surcharge – late filing fee or oath | |
| 1052 | 50 | 2052 | 25 | Surcharge – late provisional filing fee or cover sheet | |
| 1053 | 130 | 1053 | 130 | Non-English specification | |
| 1812 | 2,520 | 1812 | 2,520 | For filing a request for *ex parte* reexamination | |
| 1804 | 920* | 1804 | 920* | Requesting publication of SIR prior to Examiner action | |
| 1805 | 1,840* | 1805 | 1,840* | Requesting publication of SIR after Examiner action | |
| 1251 | 110 | 2251 | 55 | Extension for reply within first month | |
| 1252 | 420 | 2252 | 210 | Extension for reply within second month | |
| 1253 | 950 | 2253 | 475 | Extension for reply within third month | |
| 1254 | 1,480 | 2254 | 740 | Extension for reply within fourth month | |
| 1255 | 2,010 | 2255 | 1,005 | Extension for reply within fifth month | |
| 1401 | 330 | 2401 | 165 | Notice of Appeal | |
| 1402 | 330 | 2402 | 165 | Filing a brief in support of an appeal | 330.00 |
| 1403 | 290 | 2403 | 145 | Request for oral hearing | |
| 1451 | 1,510 | 1451 | 1,510 | Petition to institute a public use proceeding | |
| 1452 | 110 | 2452 | 55 | Petition to revive – unavoidable | |
| 1453 | 1,330 | 2453 | 665 | Petition to revive – unintentional | |
| 1501 | 1,330 | 2501 | 665 | Utility issue fee (or reissue) | |
| 1502 | 480 | 2502 | 240 | Design issue fee | |
| 1503 | 640 | 2503 | 320 | Plant issue fee | |
| 1460 | 130 | 1460 | 130 | Petitions to the Commissioner | |
| 1807 | 50 | 1807 | 50 | Processing fee under 37 CFR 1.17(q) | |
| 1806 | 180 | 1806 | 180 | Submission of Information Disclosure Stmt | |
| 8021 | 40 | 8021 | 40 | Recording each patent assignment per property (times number of properties) | |
| 1809 | 770 | 2809 | 385 | Filing a submission after final rejection (37 CFR 1.129(a)) | |
| 1810 | 770 | 2810 | 385 | For each additional invention to be examined (37 CFR 1.129(b)) | |
| 1801 | 770 | 2801 | 385 | Request for Continued Examination (RCE) | |
| 1802 | 900 | 1802 | 900 | Request for expedited examination of a design application | |

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid **SUBTOTAL (3)** **($)330.00**

## SUBMITTED BY

*Complete (if applicable)*

| Name (Print/Type) | Michael Farjami, Esq. | Registration No. (Attorney/Agent) | 38135 | Telephone | (949) 282-1000 |
|---|---|---|---|---|---|
| Signature | | | | Date | 7/13/04 |

**WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.**

# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | |
|---|---|
| In re Application of: | Art Unit: 2815 |
| **Han, K. Michael** | Examiner: Wojciechowicz, Edward |
| Serial No.: 09/904,042 | |
| Filed: July 11, 2001 | |
| For: **Recessed Tunnel Oxide Profile For Improved Reliability In NAND Devices** | |

## APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is an Appeal from the Examiner's Final Rejection of claims 8, 9, 14-17, and 19-22. The Final Rejection issued on February 24, 2004. The Notice of Appeal was filed in the U.S. Patent and Trademark Office on May 20, 2004.

## REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc.

## RELATED APPEALS AND INTERFERENCES

There are no related Appeals or Interferences.

## STATUS OF CLAIMS

Claims 8, 9, 14-17, and 19-22 are pending, and claims 1-7 10-13, and 18 were canceled in previous amendments. Claims 8, 9, 14-17, and 19-22 have been finally rejected in a Final Rejection dated February 24, 2004. This Appeal is directed to the rejection of claims 8, 9, 14-17, and 19-22 which appear in an Appendix to this Appeal Brief.

## STATUS OF AMENDMENTS

No claim amendments have been submitted in response to the Final Rejection of February 24, 2004.

## SUMMARY OF INVENTION

### A. Brief Description

The present invention relates to a NAND-type memory cell fabricated using controlled formation of a tunnel oxide layer to reduce oxide breakdown and/or current

leakage in the tunnel oxide layer. As disclosed in the present application, tunnel oxide layer 50 of memory cell 40 is formed over a substrate active region, which includes P-well 44 and respective source and drain regions 46 and 48, in a two step process. Page 5, lines 4-10 and Figure 2B of the present application. As disclosed in the present application, in a first step, first portion 52 of tunnel oxide layer 50 is formed over the substrate active region such that first portion 52 has thickness T, which is equal to a thickness necessary for ensuring that the injection field is such that the risk of cell failure in overlap regions 58 is reduced. Page 5, lines 10-13 and Figure 2B of the present application. By way of example, thickness T of first portion 52 may be between about 15 nm and about 30 nm. Page 5, lines 14-15 of the present application. As shown in Figure 2B, overlap regions 58 include portions of tunnel oxide layer 50 that overlap a portion of source region 46 and a portion of drain region 48. As further shown in Figure 2B, tunnel oxide layer 50 is situated over substantially less than the entire lengths of source region 46 and drain region 48.

As disclosed in the present application, in a second step in the formation of tunnel oxide layer 50, recessed portion 54 is formed into a section of tunnel oxide layer 50 that is directly over channel region 56, which is the predominant area of electron flow during the programming and erasing of the cell. Page 5, lines 21-24 and Figure 2B of the present application. As disclosed in the present application, recessed portion 54 has thickness T' over channel region 56, which is less than thickness T of first portion 52 of tunnel oxide layer 50 in overlap regions 58. Page 5, lines 32-33, page 6, lines 1-2, and Figure 2B of

the present application. By way of example, thickness T' of recessed portion 54 of tunnel oxide layer 50 over channel region 56 can be between about 4 nm and about 12 nm. Page 6, lines 1-2 of the present application.

Thus, by forming tunnel oxide layer 50 such that first portion 52 has thickness T in overlap regions 58 and recessed portion 54 has thickness T' directly over channel region 56, where thickness T is greater than thickness T', the present invention advantageously achieves a memory cell having an injection field in overlap regions, such as overlap regions 58, that is significantly lower than the injection field in the channel region, such as channel region 56. By reducing the injection field in the overlap regions, the present invention also advantageously reduces the potential for oxide breakdown and/or current leakage in the overlap regions. Page 3, lines 31-32 of the present application. Also, by making the portion of the tunnel oxide layer overlying the channel region thinner than the portion of the tunnel oxide layer in the overlap regions, the present invention advantageously ensures that a suitable injection field is attained for programming and erasing functions. Page 4, lines 1-3 of the present application.

**B. Claim 8 and its dependent claims**

The memory cell of independent claim 8 includes, among other things, a gate insulating layer (e.g. tunnel oxide layer 50) situated over an entire length of a third region (e.g. channel region 56), which is situated between first and second regions (e.g. source and drain regions 46 and 48) and which has an opposite conduction type than the first and second regions, and over substantially less than an entire length of each of the first and

second regions, where the gate insulating layer has a first thickness (e.g. thickness T) over the first and second regions and a second thickness (e.g. thickness T') over the third region, and where the first thickness is substantially uniform and the second thickness is substantially uniform, and a control gate (e.g. poly II layer 66) situated over the gate insulating layer.

Dependent claims 14 through 17 specify various embodiments of the memory cell of independent claim 8. Claim 14 specifies a first thickness of between about 20 and 30 nm and a second thickness of between about 8 and 11 nm, claim 15 specifies an injection field in an overlap region (e.g. overlap region 58) situated between the gate insulating layer and the first and second regions of between approximately 4 Mv/cm and approximately 6 Mv/cm, claim 16 specifies an injection field in an overlap region situated between the gate insulating layer and the third region of between approximately 8 Mv/cm and approximately 11 Mv/cm, and claim 17 specifies a gate insulating layer comprising $SiO_2$.

**C. Claim 9 and its dependent claims**

The memory cell of independent claim 9 includes, among other things, a gate insulating layer (e.g. tunnel oxide layer 50) situated over an entire length of a third region (e.g. channel region 56), which is situated between first and second regions (e.g. source and drain regions 46 and 48) and which has an opposite conduction type than the first and second regions, and over substantially less than an entire length of each of the first and second regions, where the gate insulating layer has a first thickness (e.g. thickness T) over

the first and second regions and a second thickness (e.g. thickness T') over the third region, and where the first thickness is substantially uniform and the second thickness is substantially uniform, and an ONO stack (e.g. ONO stack 64) situated over the gate insulating layer.

Dependent claims 19-22 specify various embodiments of the memory cell of independent claim 9. Claim 19 specifies a first thickness of between about 20 and 30 nm and a second thickness of between about 8 and 11 nm, claim 20 specifies an injection field in an overlap region (e.g. overlap region 58) situated between the gate insulating layer and the first and second regions of between approximately 4 Mv/cm and approximately 6 Mv/cm, claim 21 specifies an injection field in an overlap region situated between the gate insulating layer and the third region of between approximately 8 Mv/cm and approximately 11 Mv/cm, and claim 22 specifies a gate insulating layer comprising $SiO_2$.

## ISSUES

(1) Whether the Examiner's rejection that claims 8, 9, 17, and 22 on Appeal are unpatentable under 35 U.S.C. §102 as being anticipated by U.S. Patent No. 6,429,072 to Masaru Tsukiji ("Tsukiji") is erroneous.

(2) Whether the Examiner's rejection that claims 14-16 and 19-21 on Appeal are unpatentable under 35 U.S.C. §103 over Tsukiji and further in view of U.S. Patent No. 6,432,762 B1 to Liberia et al. ("Liberia") is erroneous.

## GROUPING OF CLAIMS

Claims 8, 9, 14-17, and 19-22 stand or fall together, for the reasons set forth in the Argument.

## ARGUMENT

### (1) The Rejection of Claims 8, 9, 17, and 22

Claims 8, 9, 17, and 22 stand rejected under 35 U.S.C. §102 as being anticipated by Tsukiji. For the reasons discussed below, Appellant respectfully submits that the present invention, as defined by independent claims 8 and 9, is patentably distinguishable over Tsukiji.

In contrast to the present invention as defined by independent claims 8 and 9, Tsukiji does not teach, disclose, or suggest a gate insulating layer situated over an entire length of a third region, which is situated between first and second regions and which has an opposite conduction type than the first and second regions, and over substantially less than an entire length of each of the first and second regions, where the gate insulating layer has a first thickness over the first and second regions and a second thickness over the third region, and where the first thickness is substantially uniform and the second thickness is substantially uniform. Tsukiji specifically discloses gate oxide film 102 situated on the top surface of the channel region of semiconductor substrate 101 and inter-layer insulators 122 situated on side walls and top surfaces of source side and drain

side interconnections 104a and 105a, which overly respective source and drain regions 104 and 105. See, for example, column 8, lines 25-26, column 9, lines 12-19, and Figure 5E of Tsukiji. In Tsukiji, inter-layer insulators 122 are thicker than gate oxide film 102. See, for example, Tsukiji, column 8, lines 1-2.

In Tsukiji, the top surface of the channel region of semiconductor substrate 101 is defined between source and drain regions 104 and 105. See, for example, Tsukiji, column 7, lines 54-57. Thus, in Tsukiji, gate oxide film 102 is situated on the top surface of the channel region of semiconductor substrate 10 and situated between source and drain regions 104 and 105. Consequently, in Tsukiji, gate oxide film 102 is not situated over a portion of source and drain regions 104 and 105. Thus, Tsukiji fails to teach, disclose, or suggest a gate insulating layer situated over an entire length of a third region, which is situated between first and second regions and which has an opposite conduction type than the first and second regions, and over substantially less than an entire length of each of the first and second regions, as specified in independent claims 8 and 9.

On page 2 of the Final Rejection dated February 24, 2004, the Examiner states that "the 'gate insulating layer' (102) in Tsukiji is situated over the entire length of the channel, and substantially less than the entire length of the source and drain regions." The Examiner further states that "the thicker parts of the gate insulating layer, which are in contact with the substrate surface, do not extend substantially over the source and drain regions." Page 2 of the Final Rejection dated February 24, 2004. However, the Examiner is equating the portion of inter-layer insulators 122 that is situated on semiconductor

substrate 101, i.e. the portion of inter-layer insulators 122 that is situated on the side walls of source side and drain side interconnections 104a and 105a, with gate oxide film 102, which is situated on the top surface of the channel region of semiconductor substrate 10. Appellant respectfully submits that inter-layer insulators 122 and gate oxide film 102 are different layers.

Assuming, arguendo, that inter-layer insulators 122 and gate oxide film 102 are a single "gate insulating layer." The "gate insulating layer" would extend over a substantial portion of source and drain regions 104 and 105, since inter-layer insulators 122 are situated on the top surfaces of source side and drain side interconnections 104a and 105a, which overly respective source and drain regions 104 and 105. However, the Examiner conveniently calls gate oxide film 102 and portions of inter-layer insulators 122 situated on semiconductor substrate 101 a "gate insulating layer" while excluding the portions of inter-layer insulators 122 that are situated over a substantial portion of source and drain regions 104 and 105.

Thus, in Tsukiji, if inter-layer insulators 122 and gate oxide film 102 are considered as separate layers, gate oxide film 102 is not situated over a portion of source and drain regions 104 and 105, since gate oxide film 102 is situated between source and drain regions 104 and 105. Alternatively, if inter-layer insulators 122 and gate oxide film 102 are considered a single "gate insulating layer," then the "gate insulating layer" is situated over a substantial portion of source and drain regions 104 and 105, since inter-layer insulators 122 are situated over a substantial portion of source and drain regions 104

and 105. Thus, Tsukiji fails to teach, disclose, or suggest a gate insulating layer situated over an entire length of a third region, which is situated between first and second regions and which has an opposite conduction type than the first and second regions, and over substantially less than an entire length of each of the first and second regions, where the gate insulating layer has a first thickness over the first and second regions and a second thickness over the third region, as specified in independent claims 8 and 9.

For the foregoing reasons, Appellant respectfully submits that the present invention, as disclosed by independent claims 8 and 9, is not suggested, disclosed, or taught by Tsukiji. As such, the present invention, as defined by independent claims 8 and 9, is patentably distinguishable over Tsukiji. Thus, claim 17 depending from independent claim 8 and claim 22 depending form independent claim 9 are, *a fortiori*, also patentably distinguishable over Tsukiji for at least the reasons presented above and also for additional limitations contained in each dependent claim.

**(2) <u>The Rejection of Claims 14-16 and 19-21</u>**

Claims 14-16 and 19-21 stand rejected under 35 U.S.C. §103 as being unpatentable over Tsukiji and further in view of Liberia. As discussed above, the present invention, as defined by independent claims 8 and 9, is patentably distinguishable over Tsukiji. Thus, claims 14-16 depending from independent claim 8 and claims 19-21 depending from independent claim 9 are, *a fortiori*, also patentably distinguishable over

Tsukiji for at least the reasons presented above and also for additional limitations contained in each dependent claim.

## CONCLUSION

Based on the foregoing reasons, the present invention, as defined by independent claims 8 and 9 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 8, 9, 14-17, and 19-22 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 8, 9, 14-17, and 19-22 pending in the present application is respectfully requested.

This Appeal Brief is submitted herewith in triplicate along with an Appendix of the appealed claims and the requisite fee for filing the Appeal Brief.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 7/13/04

Michael Farjami, Esq.
Reg. No. 38, 135

FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, California 92691
Telephone: (949) 282-1000
Facsimile: (949) 282-1002

*CERTIFICATE OF FACSIMILE TRANSMISSION*
I hereby certify that this correspondence is being filed by facsimile transmission to United States Patent and Trademark Office at facsimile number **703-872-9306** on the date stated below. The facsimile transmission report indicated that the facsimile transmission was successful.

Date of Facsimile:_____

_____
Name of Person Performing Facsimile Transmission

_____
Signature Date

*CERTIFICATE OF MAILING*
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed: Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Date of Deposit: 7-13-04

Susan Hanson
Name of Person Mailing Paper and/or Fee

Susan Hanson 7-13-04
Signature Date

## APPENDIX OF CLAIMS ON APPEAL

**Claim 8:** A memory cell comprising:

a semiconductor substrate having a first region and a second region of one conduction type and a third region therebetween of an opposite conduction type;

a gate insulating layer situated over an entire length of said third region and substantially less than an entire length of each of said first region and said second region, the gate insulating layer having a first thickness situated over said first region and said second region, and a second thickness situated over said third region, said first thickness being greater than said second thickness, wherein said first thickness is substantially uniform and said second thickness is substantially uniform; and

a control gate situated over said gate insulating layer.

**Claim 9:** A memory cell comprising:

a semiconductor substrate having a first region and a second region of one conduction type and a third region therebetween of an opposite conduction type; and

a gate insulating layer situated over an entire length of said third region and substantially less than an entire length of each of said first region and said second region, the gate insulating layer having a first thickness situated over said first region and said second region, and a second thickness situated over said third region, said first thickness

being greater than said second thickness, wherein said first thickness is substantially uniform and said second thickness is substantially uniform; and

an ONO stack situated over said gate insulating layer.

**Claim 14:** A memory cell as in claim 8, wherein said first thickness is between about 20 and 30 nm and wherein said second thickness is between about 8 and 11 nm.

**Claim 15:** A memory cell as in claim 8, wherein an injection field in an overlap region situated between said gate insulating layer and said first and second regions ranges between approximately 4 Mv/cm and approximately 6 Mv/cm.

**Claim 16:** A memory cell as in claim 8, wherein an injection field in an overlap region situated between said gate insulating layer and said third region ranges between approximately 8 Mv/cm and approximately 11 Mv/cm.

**Claim 17:** A memory cell as in claim 8, wherein said gate insulating layer comprises $SiO_2$.

**Claim 19:** A memory cell as in claim 9, wherein said first thickness is between about 20 and 30 nm and wherein said second thickness is between about 8 and 11 nm.

**Claim 20:** A memory cell as in claim 9, wherein an injection field in an overlap region situated between said gate insulating layer and said first and second regions ranges between approximately 4 Mv/cm and approximately 6 Mv/cm.

**Claim 21:** A memory cell as in claim 9, wherein an injection field in an overlap region situated between said gate insulating layer and said third region ranges between approximately 8 Mv/cm and approximately 11 Mv/cm.

**Claim 22:** A memory cell as in claim 9, wherein said gate insulating layer comprises $SiO_2$.